

SPICE model of memristive devices with threshold

Yuriy V. Pershin and Massimiliano Di Ventra

Abstract—Although memristive devices with threshold voltages are the norm rather than the exception in experimentally realizable systems, their SPICE programming is not yet common. Here, we show how to implement such systems in the SPICE environment. Specifically, we present SPICE models of a popular voltage-controlled memristive system specified by five different parameters for PSPICE and NGSPICE circuit simulators. We expect this implementation to find widespread use in circuits design and testing.

Index Terms—Memristive devices, memristor, memristor model, threshold dynamics.

I. INTRODUCTION

IN the last few years, circuit elements with memory, namely, memristive [1], memcapacitive and meminductive [2] systems have attracted considerable attention from different disciplines due to their capability to store and manipulate information on the same physical platform [3]. However, when combined into complex circuits, progress in this field significantly relies on the available tools at our disposal. One such tool is the SPICE simulation environment, commonly used in circuit simulations and testing. While several SPICE models of memristive [4], [5], [6], [7], [8], [9], [10], memcapacitive [6] and meminductive [6] elements are already available, they typically [4], [5], [6], [7], [8] rely on physical models without a threshold (see, e.g., Refs. [11], [12]).

Threshold-type switching is instead an extremely important common feature of memristive devices (for examples, see Ref. [3]) and, due to physical constraints, likely to be common in memcapacitive and meminductive elements as well. Indeed, it is the threshold-type switching which is responsible for non-volatile information storage, serves as a basis for logic operations [13], [14], etc., and therefore, it can not be neglected.

In the present paper we introduce a SPICE model for a memristive device with threshold voltage that has been proposed by the present authors [15]. Using this type of memristive devices, we have already demonstrated and analyzed several electronic circuits including a learning circuit [15], memristive neural networks [16], logic circuits [14], analog circuits [17] and circuits transforming memristive response into memcapacitive and meminductive ones [18]. These previous results thus demonstrate the range of applicability of the selected physical model. As a consequence, we expect its SPICE implementation to find numerous applications as well.

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Manuscript received May XX, 2012; revised June YY, 2012.

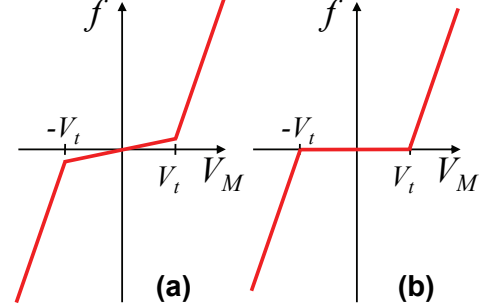


Fig. 1. Sketch of the function $f(V_M)$ for (a) $\alpha > 0$ and $\beta > 0$ and (b) $\alpha = 0$ and $\beta > 0$.

II. SPICE MODEL

The equations describing memristive systems can be formulated in the voltage- or current-controlled form [1]. In some cases, a voltage-controlled memristive system can be easily re-formulated as a current-controlled one and vice versa [3]. Let us then focus on voltage-controlled memristive systems whose general definition (for an n th-order voltage-controlled memristive system) is given by the following relations

$$I(t) = R_M^{-1}(X, V_M, t) V_M(t), \quad (1)$$

$$\dot{X} = f(X, V_M, t) \quad (2)$$

where X is the vector representing n internal state variables, $V_M(t)$ and $I(t)$ denote the voltage and current across the device, and R_M is a scalar, called the *memristance* (for memory resistance).

A specific realization of a voltage-controlled memristive system *with threshold* has been suggested by the present authors in Ref. [15]. Such a memristive system is described

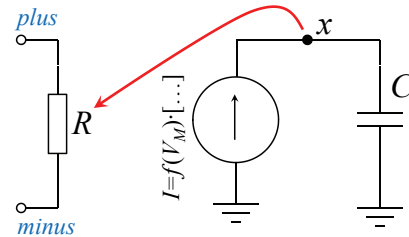


Fig. 2. Schematic of the SPICE model. The memristive device functionality is organized as a subcircuit consisting of a behavioral resistor R , current source \uparrow and capacitor C . The voltage across the capacitor (at the node x) defines the resistance of R .

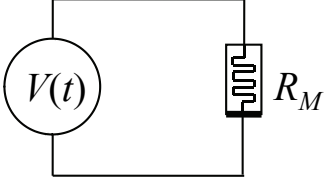


Fig. 3. Memristive device directly connected to a voltage source $V(t)$.

by

$$I = X^{-1}V_M, \quad (3)$$

$$\frac{dX}{dt} = f(V_M) [\theta(V_M) \theta(R_{off} - X) + \theta(-V_M) \theta(X - R_{on})], \quad (4)$$

with

$$f(V_M) = \beta V_M + 0.5(\alpha - \beta) [|V_M + V_t| - |V_M - V_t|], \quad (5)$$

where V_t is the threshold voltage, R_{on} and R_{off} are limiting values of the memristance $R_M \equiv X$, and the θ -functions (step functions) are used to limit the memristance to the region between R_{on} and R_{off} . The important model parameters are the coefficients α and β that characterize the rate of memristance change at $|V_M| < V_t$ and $|V_M| > V_t$, respectively. These two coefficients define the slopes of the $f(V_M)$ curve below and above the threshold (see Fig. 1). When $\alpha = 0$ (Fig. 1(b)), the device state changes only if $|V_M| > V_t$. Note that Eqs. (3)-(5) are written in such a way that a positive/negative voltage applied to the top terminal with respect to the bottom terminal denoted by the black thick line always tends to increase/decrease the memristance R_M (the opposite convention has been used in Ref. [15]).

The SPICE model for these devices is formulated following the general idea of Ref. [4]. For NGSPICE circuit simulator, the memristive system is realized as a sub-circuit combining a behavioral resistor R (a resistor whose resistance can be specified by an expression), a current source \uparrow , and a capacitor C . Table I presents the code of the sub-circuit. Its second line (*Bx ...*) defines the current source with the current specified through ternary functions. (A ternary function is defined in the code as $a ? b : c$, which means "IF a, THEN b, ELSE c" [19].) The purpose of these functions is to limit R_M between R_{on} and R_{off} . The third line of the code in Table I specifies the capacitor C (*Cx ...*) with an initial condition. The fourth line (*Rmem ...*) defines the behavioral resistor whose resistance takes the same numerical value as the voltage across the capacitor. The next line (*func ...*) provides the function f according to Eq. (5).

For PSPICE circuit simulator, the SPICE model of memristive device with threshold is formulated slightly differently without the use of behavioral resistor. Instead, we employ an additional current source playing the role of behavioral resistor [20]. In addition, in order to avoid convergence problems, the function f in Eq. (5) should be smoothed. In the most important case of $\alpha = 0$, the smoothing of f is straightforward. Table II presents the code for PSPICE circuit simulator for this

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.subckt memristor plus minus PARAMS: Ron=1K Roff=10K Rinit=5K
alpha=0 beta=1E13 Vt=4.6
Bx 0 x I={f1(V(plus)-V(minus))>0} && (V(x)<Roff) ? {f1(V(plus)-
V(minus))}: {f1(V(plus)-V(minus))<0} && (V(x)>Ron) ? {f1(V(plus)-
V(minus))}: {0}'
Cx x 0 1 IC={Rinit}
Rmem plus minus r={V(x)}
.func f1(y)={beta*y+0.5*(alpha-beta)*(abs(y+Vt)-abs(y-Vt))}
.ends
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TABLE I
NGSPICE IMPLEMENTATION OF Eqs. (3)-(5).

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.subckt memristor pl mn PARAMS: Ron=1K Roff=10K Rinit=5K
beta=1E13 Vt=4.6 nu1=0.0001 nu2=0.1
Gx 0 x value={f1(V(pl)-V(mn))*(f2(f1(V(pl)-V(mn)))*f3(Roff-V(x))+f2(-
f1(V(pl)-V(mn)))*f3(V(x)-Ron))}
Raux x 0 1E12
Cx x 0 1 IC={Rinit}
Gpm pl mn value={(V(pl)-V(mn))/V(x)}
.func f1(y)={beta*(y-Vt)*f2(y-Vt)+beta*(y+Vt)*f2(-y-Vt)}
.func f2(y)={1/(exp(-y/nu1)+1)}
.func f3(y)={1/(exp(-y/nu2)+1)}
.ends
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TABLE II
PSPICE IMPLEMENTATION OF Eqs. (3)-(5) FOR $\alpha = 0$.

case. In Table II, $nu1$ and $nu2$ are smoothing parameters used in smoothed step functions $f2$ and $f3$ (although we prefer to use different smoothing parameters for functions of voltages and resistances, a common smoothing function could also be used). We have verified that simulation results are identical in both versions of SPICE.

III. EXAMPLE

Let us consider a memristive device with threshold directly connected to a sinusoidal voltage source $V(t) = V_0 \sin(2\pi\nu t)$ as presented in Fig. 3. The circuit simulations are performed as a transient analysis of the circuit taking into account initial conditions (the *uic* option of *.tran*) within the NGSPICE circuit simulator. In our simulations, we consider two different types of memristive devices with threshold corresponding to two cases of functions $f(V_M)$ as presented in Fig. 1. In the first case (that can be dubbed as a memristive device with a "soft" threshold) the coefficients $\alpha, \beta > 0$ and $\alpha < \beta$. In this case, the memristance changes at any $V \neq 0$. However, the change is faster when the applied voltage magnitude is above the threshold voltage ($|V| > V_t$). In the second case (Fig. 1(b)), $\alpha = 0$. Consequently, the memristance changes only when the applied voltage exceeds the threshold voltage ($|V| > V_t$). This second case is closer to the actual behavior of many experimentally realizable memristive systems [3]. We call this type of systems as memristive devices with "hard" threshold.

Fig. 4 presents selected results of our simulations showing the circuit dynamics at long times (the initial transient interval

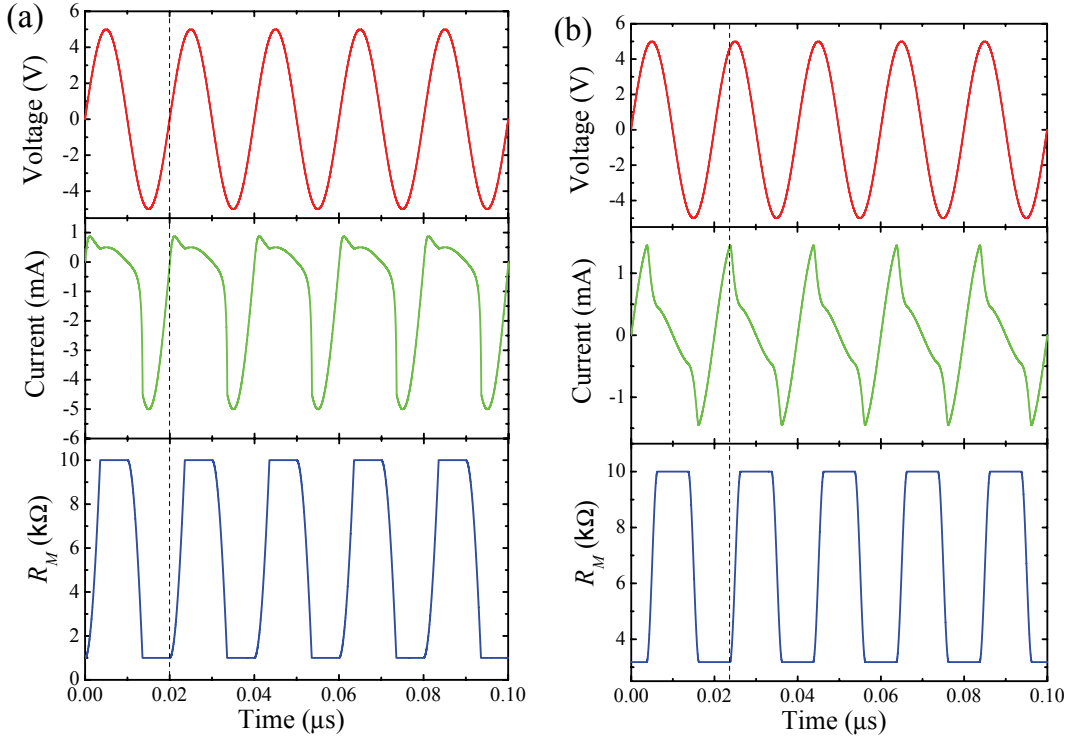


Fig. 4. Time evolution of the applied voltage $V(t)$, current $I(t)$ and memristance $R_M(t)$ for memristive devices with (a) soft ($\alpha = 0.1\beta$), and (b) hard ($\alpha = 0$) thresholds. The vertical dashed lines - corresponding to the onset of switching - serve as guide to the eye. The simulations parameters are as follows: the applied voltage amplitude $V_0 = 5\text{V}$, $\nu = 0.05\text{GHz}$, $R_{on} = 1\text{k}\Omega$, $R_{off} = 10\text{k}\Omega$, $R_M(t=0) = 5\text{k}\Omega$, $\beta = 10^{10}\text{k}\Omega/(\text{V s})$, $V_t = 4.6\text{V}$.

is omitted). We consider two types of memristive devices – one with a soft and another with hard thresholds ($\alpha = 0.1\beta$ and $\alpha = 0$, respectively) – and plot the applied voltage, current and memristance as functions of time for these two cases at a frequency $\nu = 0.05\text{GHz}$. Clearly, in both cases, the current through the device is not of the simple sine form. The plot of memristance as a function of time demonstrates that the range of memristance change in (a) is larger than in (b) (actually, in (a), R_M switches between R_{on} and R_{off}). The vertical dashed line in Fig. 4(a) helps noticing that in Fig. 4(a) the memristance starts changing as soon as the sign of applied voltage changes. In Fig. 4(b), instead, the change of R_M occurs solely when $|V| > V_t$. As a consequence, the shapes of $R_M(t)$ in Fig. 4(a) and (b) are slightly different, and the steps in $R_M(t)$ in Fig. 4(b) are shifted along the horizontal axis compared to those in Fig. 4(a).

The current as a function of voltage at several selected values of ν is plotted in Fig. 5. Clearly, these curves are typical frequency-dependent pinched hysteresis loops [1], [2]. The character of the loops for memristive systems with hard and soft thresholds is slightly different. While for memristive systems with soft threshold the curve for the lowest frequency has the smallest loop span, the situation for the memristive system with hard threshold is opposite: the largest loop span occurs at the lowest frequency. This result, however, is not surprising if we take into account the fact that in the memristive system with soft threshold the change of R_M occurs at lower voltages. Moreover, the insets of Fig. 5 demonstrate

the memristance $R_M(t)$ as a function of $V(t)$ at a particular frequency. It is not difficult to notice that in the case of the memristive system with hard threshold (shown in the inset of Fig. 5(b)), R_M changes only when $|V|$ exceeds $V_t = 4.6\text{V}$.

IV. CONCLUSIONS

We have developed and tested a SPICE model of memristive devices with threshold voltage. In this model, the limiting conditions for the memristance are realized using ternary functions which adhere more closely to the actual physical situation, compared with the window functions approach previously suggested [12]. The memristive device is realized as a sub-circuit consisting of several elements. While the present model is based on a single internal state variable, X , it can be easily generalized to more complex physical models involving several internal state variables. Finally, we note that threshold models of memcapacitive and meminductive systems can be implemented in the SPICE environment in a similar way.

ACKNOWLEDGMENT

M.D. acknowledges partial support from the National Science Foundation (DMR-0802830).

REFERENCES

- [1] L. O. Chua and S. M. Kang, “Memristive devices and systems,” *Proc. IEEE*, vol. 64, pp. 209–223, 1976.
- [2] M. Di Ventra, Y. V. Pershin, and L. O. Chua, “Circuit elements with memory: Memristors, memcapacitors, and meminductors,” *Proc. IEEE*, vol. 97, no. 10, pp. 1717–1724, 2009.

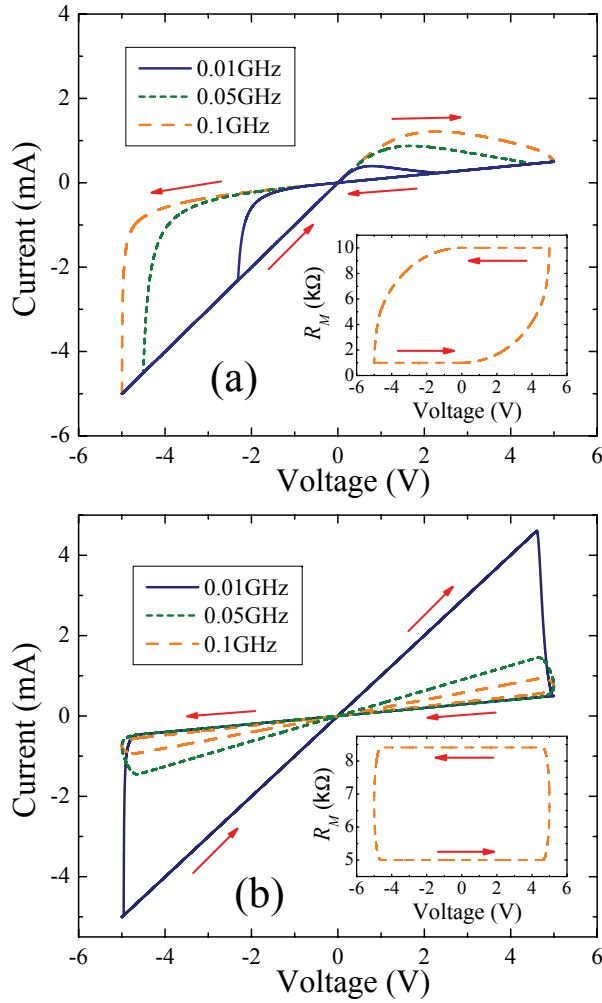


Fig. 5. Frequency-dependent hysteresis loops for memristive devices with soft (a) and hard (b) thresholds. The simulations parameters are as in Fig. 4 except of ν . The applied voltage frequencies ν are indicated on the plots. The insets (calculated at 0.1GHz sine voltage frequency) show the memristance as a function of applied voltage. The inset in (b) demonstrates that in the case of the hard threshold the memristance changes only when the absolute value of the applied voltage exceeds the threshold voltage V_t .

- [11] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.
- [12] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *Eur. J. Phys.*, vol. 30, p. 661, 2009.
- [13] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, pp. 873–876, 2010.
- [14] Y. V. Pershin and M. Di Ventra, "Neuromorphic, digital and quantum computation with memory circuit elements," *Proc. IEEE*, vol. 100, p. 2071, 2012.
- [15] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, "Memristive model of amoeba learning," *Phys. Rev. E*, vol. 80, p. 021926, 2009.
- [16] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Networks*, vol. 23, p. 881, 2010.
- [17] —, "Practical approach to programmable analog circuits with memristors," *IEEE Trans. Circ. Syst. I*, vol. 57, p. 1857, 2010.
- [18] —, "Memristive circuits simulate memcapacitors and meminductors," *Electronics Letters*, vol. 46, pp. 517–518, 2010.
- [19] P. Nenzi and H. Vogt. (2012) Ngspice users manual. [Online]. Available: <http://ngspice.sourceforge.net/docs/ngspice-manual.pdf>
- [20] C. Basso, "SPICE analog behavioral modeling of variable passives," *Power Electronics Technology*, pp. 57–59, April 2005.

- [3] Y. V. Pershin and M. Di Ventra, "Memory effects in complex materials and nanoscale systems," *Advances in Physics*, vol. 60, pp. 145–227, 2011.
- [4] Z. Biolek, D. Biolek, and V. Biolkova, "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, Part 2, pp. 210–214, 2009.
- [5] S. Benderli and T. A. Wey, "On SPICE macromodelling of TiO₂ memristors," *Electron. Lett.*, vol. 45, no. 7, pp. 377–378, 2009.
- [6] Z. Biolek, D. Biolek, and V. Biolkova, "SPICE modeling of memristive, memcapacitive and meminductive systems," *Proc. of ECCTD '09, European Conference on Circuit Theory and Design*, pp. 249–252, August 23–27, 2009.
- [7] S. Shin, K. Kim, and S.-M. Kang, "Compact models for memristors based on charge-flux constitutive relationships," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, p. 590, 2010.
- [8] A. Rak and G. Cserey, "Macromodeling of the memristor in SPICE," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, p. 632, 2010.
- [9] C. Yakopcic, T. M. Taha, G. Subramanyam, R. E. Pino, and S. Rogers, "A memristor device model," *IEEE El. Dev. Lett.*, vol. 32, p. 1436, 2011.
- [10] S. Kvaterny, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Trans. Circ. Syst. I (in press)*, 2012.